In re Patent Application of:
WRIGHT ET AL
Serial No. **10/040,153**
Filed: **JANUARY 2, 2002**

In the Claims:

1. (original) For use with a receiver of a digital communication system, said receiver having a cell delineation mechanism that is operative, given knowledge of boundaries of respective bytes of an incoming serial data stream, to delineate respective cells of said serial data stream, a mechanism for locating said boundaries of respective bytes of said incoming serial data stream comprising:

a counter that is operative to count respective clock signals associated with said incoming serial data stream; and

a synchronization signal derivation unit, coupled to said counter and being operative to generate an output signal in potential alignment with the boundary of a byte of said incoming serial data stream, in response to contents of said counter reaching a prescribed count value, and iteratively shifting, as necessary, the time at which said output signal is produced relative to the counting operation of said counter, until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

2. (original) The mechanism according to claim 1, wherein said counter is operative to repetitively count toward said prescribed count value from a first preloaded count value, and wherein said synchronization signal derivation unit is operative to controllably program said counter with a second preloaded

count value, different from said first preloaded count value, based upon whether or not said output signal is aligned with said boundary of a byte of said incoming serial data stream.

3. (original) The mechanism according to claim 2, wherein said synchronization signal derivation unit is operative to iteratively program said counter with said second count value for an individual one or more count cycles, separated from one another by plural count cycles during which said counter is programmed to count from said first preloaded count value, until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

4. (original) The mechanism according to claim 1, wherein said counter is operative to generate an intermediate frame sync signal FS0 in response to contents thereof reaching a prescribed count value, and wherein said synchronization signal derivation unit includes a shift register to which said intermediate frame sync signal FS0 is serially shifted, and wherein said output signal is derived from a selected stage of said shift register.

5. (original) The mechanism according to claim 4, wherein said synchronization signal derivation unit is operative to controllably change the stage of said shift register from which said output signal is derived in a manner that causes said output

signal to be aligned with said boundary of a byte of said incoming serial data stream.

6. (original) The mechanism according to claim 5, wherein said synchronization signal derivation unit is operative to iteratively and successively change the stage of said shift register from which said output signal is derived over successive intervals, until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

7. (currently amended) A method for locating boundaries of respective bytes of an incoming serial data stream coupled to a receiver of a digital communication system, said receiver having a cell delineation mechanism that is operative, given knowledge of said boundaries of said respective bytes of said incoming serial data stream, to delineate respective cells of said serial data stream, said method comprising the steps of:

(a) counting respective clock signals associated with said incoming serial data stream;

(b) in response to the number of clock signals counted in step (a) reaching a prescribed count value, generating an output signal in potential alignment with the boundary of a byte of said incoming serial data stream; and

(c) iteratively adjusting as necessary, the time at which said output signal is produced in step [[(c)]] (b) relative

to the counting operation carried out in step (a), until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

8. (original) The method according to claim 7, wherein step (a) comprises repetitively counting toward said prescribed count value from a first count value, and wherein step (c) comprises controllably changing said first count value to a second count value, based upon whether or not said output signal is aligned with said boundary of a byte of said incoming serial data stream.

9. (original) The method according to claim 8, wherein step (c) comprises iteratively causing step (a) to start counting from said second count value for an individual one or more count cycles, separated from one another by plural count cycles during which step (a) counts from said first count value, until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

10. (original) The method according to claim 7, wherein step (a) comprises generating an intermediate frame sync signal FS0 in response to counting prescribed number of clock signals, said intermediate frame sync signal FS0 being shifted through a multi-stage shift register, step (b) comprises deriving said output signal from a selected stage of said shift register, and wherein

step (c) comprises controllably changing the stage of said shift register from which said output signal is derived in a manner that causes said output signal to be aligned with said boundary of a byte of said incoming serial data stream.

11. (original) The method according to claim 10, wherein step (c) comprises iteratively and successively changing the stage of said shift register from which said output signal is derived over successive intervals, until said output signal is aligned with said boundary of a byte of said incoming serial data stream.

12. (currently amended) A method of identifying initial bits within respective bytes of an incoming asynchronous transfer mode (ATM) data stream that is coupled to a receiver of a digital communication system, said receiver having a cell delineation mechanism that is operative, given knowledge of the locations of said initial bits, to delineate respective cells of said ATM data stream, said method comprising the steps of:

(a) counting respective clock signals associated with respective bits of said incoming ATM data stream;

(b) in response to the number of clock signals counted in step (a) reaching a prescribed count value, generating an output signal in potential alignment with a first bit of a byte of said incoming ATM data stream; and

(c) iteratively shifting as necessary, in a bit-wise manner, the bit time at which said output signal is produced in step [[(c)]](b) relative to the counting operation carried out in step (a), until said output signal is aligned with a first bit of a byte of said incoming ATM data stream.

13. (original) The method according to claim 12, wherein step (a) comprises repetitively counting toward said prescribed count value from a first count value, and wherein step (c) comprises controllably changing said first count value to a second count value, based upon whether or not said output signal is aligned with said first bit of a byte of said incoming ATM data stream.

14. (original) The method according to claim 13, wherein step (c) comprises iteratively causing step (a) to start counting from said second count value for an individual one or more count cycles, separated from one another by plural count cycles during which step (a) counts from said first count value, until said output signal is aligned with said first bit of a byte of said incoming ATM data stream.

15. (original) The method according to claim 14, wherein step (a) comprises generating an intermediate frame sync signal FS0 in response to counting prescribed number of clock signals,

said intermediate frame sync signal FS0 being shifted through a multi-stage shift register, step (b) comprises deriving said output signal from a selected stage of said shift register, and wherein step (c) comprises controllably changing the stage of said shift register from which said output signal is derived in a manner that causes said output signal to be aligned with said first bit of a byte of said incoming ATM data stream.

16. (original) The method according to claim 15, wherein step (c) comprises iteratively and successively changing the stage of said shift register from which said output signal is derived over successive intervals, until said output signal is aligned with said first bit of a byte of said incoming ATM data stream.